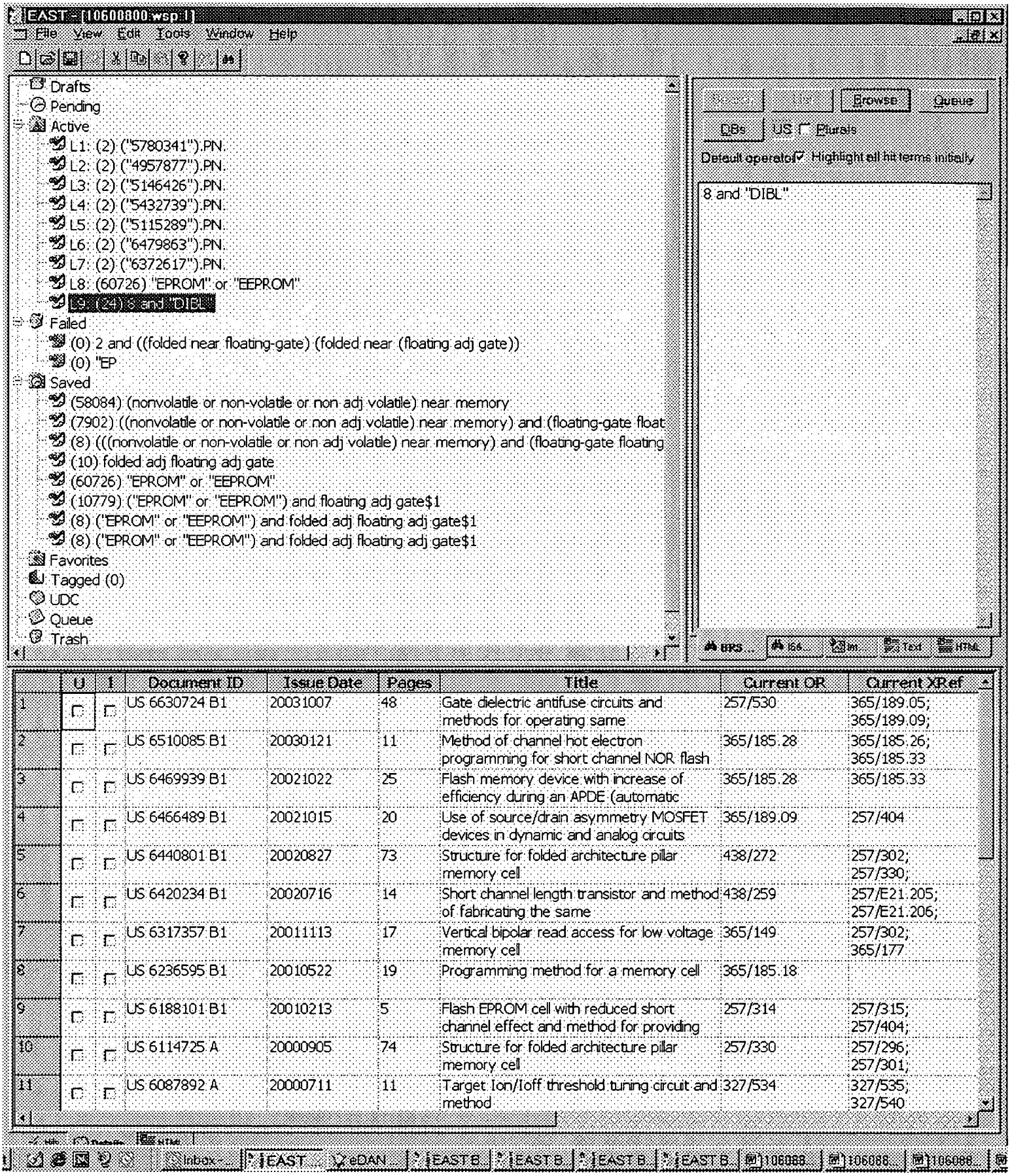

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6630724 B1	20031007	48	Gate dielectric antifuse circuits and methods for operating same	257/530	365/189.05; 365/189.09;
2	☐	☐	US 6510085 B1	20030121	11	Method of channel hot electron programming for short channel NOR flash	365/185.28	365/185.26; 365/185.33
3	☐	☐	US 6469939 B1	20021022	25	Flash memory device with increase of efficiency during an APDE (automatic	365/185.28	365/185.33
4	☐	☐	US 6466489 B1	20021015	20	Use of source/drain asymmetry MOSFET devices in dynamic and analog circuits	365/189.09	257/404
5	☐	☐	US 6440801 B1	20020827	73	Structure for folded architecture pillar memory cell	438/272	257/302; 257/330;
6	☐	☐	US 6420234 B1	20020716	14	Short channel length transistor and method of fabricating the same	438/259	257/E21.205; 257/E21.206;
7	☐	☐	US 6317357 B1	20011113	17	Vertical bipolar read access for low voltage memory cell	365/149	257/302; 365/177
8	☐	☐	US 6236595 B1	20010522	19	Programming method for a memory cell	365/185.18	
9	☐	☐	US 6188101 B1	20010213	5	Flash EPROM cell with reduced short channel effect and method for providing	257/314	257/315; 257/404;
10	☐	☐	US 6114725 A	20000905	74	Structure for folded architecture pillar memory cell	257/330	257/296; 257/301;
11	☐	☐	US 6087892 A	20000711	11	Target Ion/Ioff threshold tuning circuit and method	327/534	327/535; 327/540